



# CEP13N5/CEB13N5

## CEF13N5

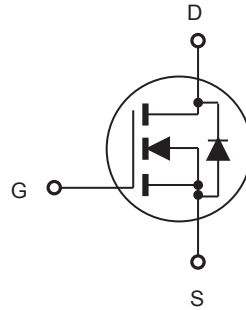
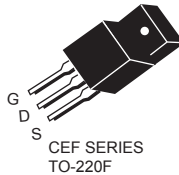
### N-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

### FEATURES

Type	V <sub>DSS</sub>	R <sub>DS(ON)</sub>	I <sub>D</sub>	@V <sub>GS</sub>
CEP13N5	500V	0.48Ω	13A	10V
CEB13N5	500V	0.48Ω	13A	10V
CEF13N5	500V	0.48Ω	13A <sup>d</sup>	10V

- Super high dense cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability.
- Lead free product is acquired.



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V <sub>DS</sub>	500		V
Gate-Source Voltage	V <sub>GS</sub>	±30		V
Drain Current-Continuous @ T <sub>C</sub> = 25°C	I <sub>D</sub>	13	13 <sup>d</sup>	A
Drain Current-Continuous @ T <sub>C</sub> = 100°C	I <sub>D</sub>	8	8 <sup>d</sup>	A
Drain Current-Pulsed <sup>a</sup>	I <sub>DM</sub> <sup>e</sup>	52	52 <sup>d</sup>	A
Maximum Power Dissipation @ T <sub>C</sub> = 25°C - Derate above 25°C	P <sub>D</sub>	214	60	W
		1.43	0.4	W/°C
Operating and Store Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 175		°C

### Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	0.7	2.5	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	65	°C/W

This is preliminary information on a new product in development now .  
Details are subject to change without notice .

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<http://www.cetsemi.com>



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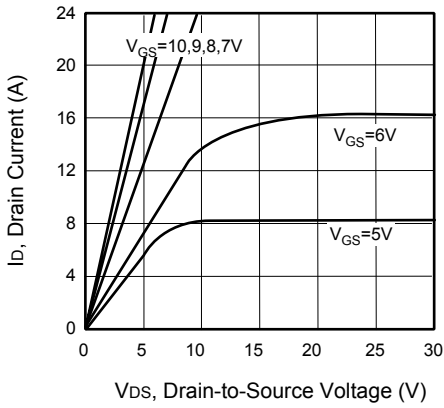
## CEF13N5

### Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

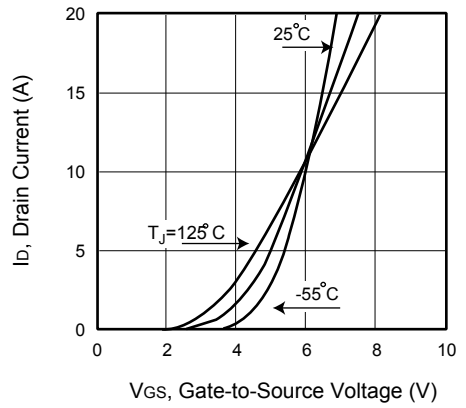
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	500			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
<b>On Characteristics <sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 6.5A$		0.38	0.48	$\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = 25V, I_D = 6.5A$		10		S
<b>Dynamic Characteristics <sup>c</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0\text{ MHz}$		2100		pF
Output Capacitance	$C_{oss}$			220		pF
Reverse Transfer Capacitance	$C_{rss}$			7		pF
<b>Switching Characteristics <sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250V, I_D = 13A, V_{GS} = 10V, R_{GEN} = 25\Omega$		42	84	ns
Turn-On Rise Time	$t_r$			62	124	ns
Turn-Off Delay Time	$t_{d(off)}$			130	260	ns
Turn-Off Fall Time	$t_f$			25	50	ns
Total Gate Charge	$Q_g$	$V_{DS} = 400V, I_D = 13A, V_{GS} = 10V$		50	66	nC
Gate-Source Charge	$Q_{gs}$			11		nC
Gate-Drain Charge	$Q_{gd}$			19		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S^f$				13	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}^g$	$V_{GS} = 0V, I_S = 13A$			1.4	V
<b>Notes :</b> a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . c.Guaranteed by design, not subject to production testing. d.Limited only by maximum temperature allowed . e.Pulse width limited by safe operating area . f.Full package $I_{S(max)} = 6.6A$ . g.Full package $V_{SD}$ test condition $I_S = 6.6A$ .						



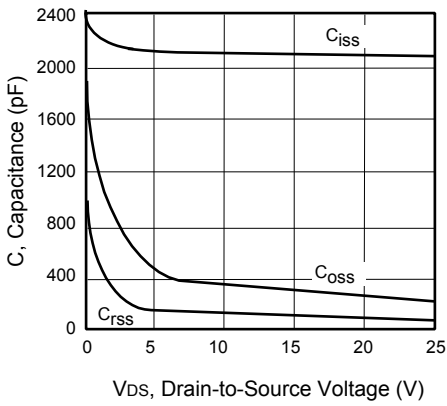
# CEP13N5/CEB13N5 CEF13N5



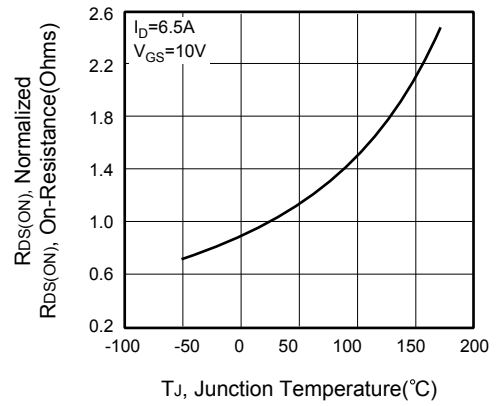
**Figure 1. Output Characteristics**



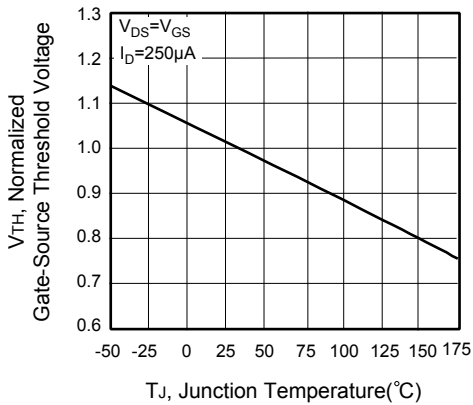
**Figure 2. Transfer Characteristics**



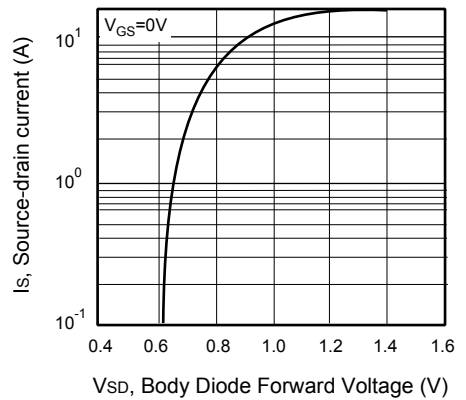
**Figure 3. Capacitance**



**Figure 4. On-Resistance Variation with Temperature**



**Figure 5. Gate Threshold Variation with Temperature**



**Figure 6. Body Diode Forward Voltage Variation with Source Current**



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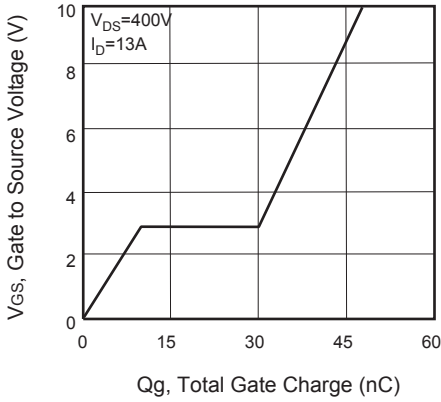


Figure 7. Gate Charge

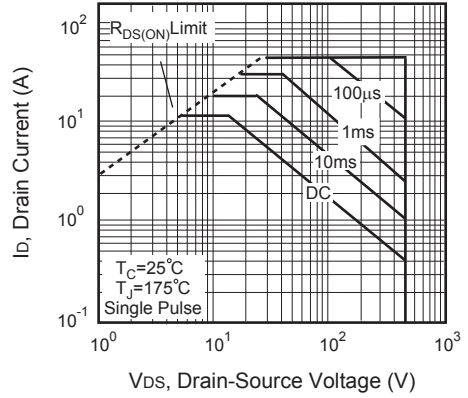


Figure 8. Maximum Safe Operating Area

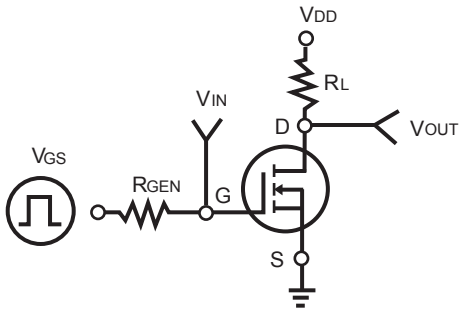


Figure 9. Switching Test Circuit

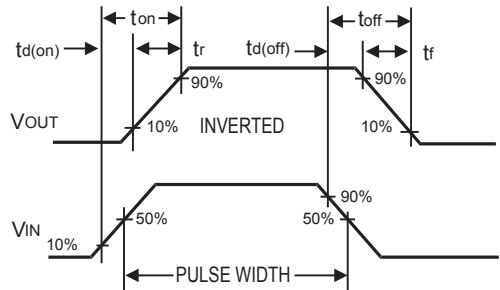


Figure 10. Switching Waveforms

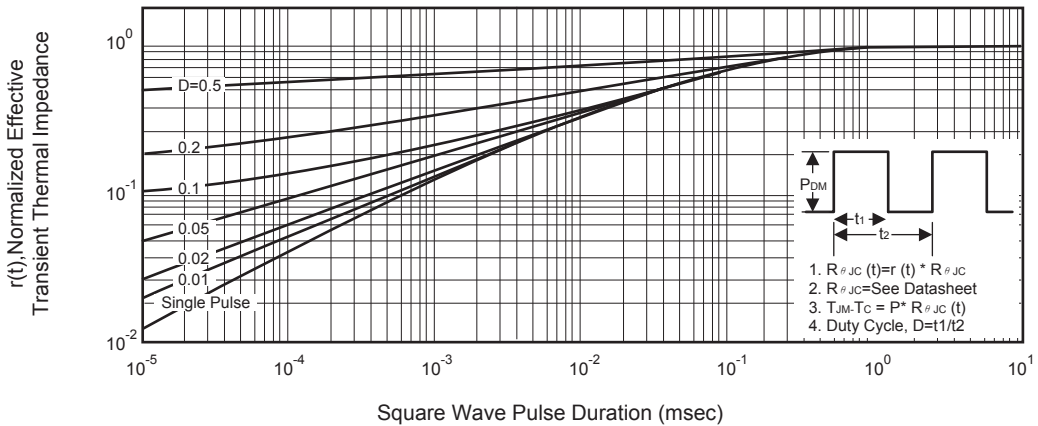


Figure 11. Normalized Thermal Transient Impedance Curve